

LMC568 Low Power Phase-Locked Loop

Check for Samples: [LMC568](#)

FEATURES

- Demodulates $\pm 15\%$ Deviation FM/FSK Signals
- Carrier Detect Output with Hysteresis
- Operation to 500 kHz Input Frequency
- Low THD—0.5% Typ. for $\pm 10\%$ Deviation
- 2V to 9V Supply Voltage Range
- Low Supply Current Drain

DESCRIPTION

The LMC568 is an amplitude-linear phase-locked loop consisting of a linear VCO, fully balanced phase detectors, and a carrier detect output. LCMOS technology is employed for high performance with low power consumption.

The VCO has a linearized control range of $\pm 30\%$ to allow demodulation of FM and FSK signals. Carrier detect is indicated when the PLL is locked to an input signal greater than 26 mVrms. LMC568 applications include FM SCA and TV second audio program decoders, FSK data demodulators, and voice pagers.

Typical Application

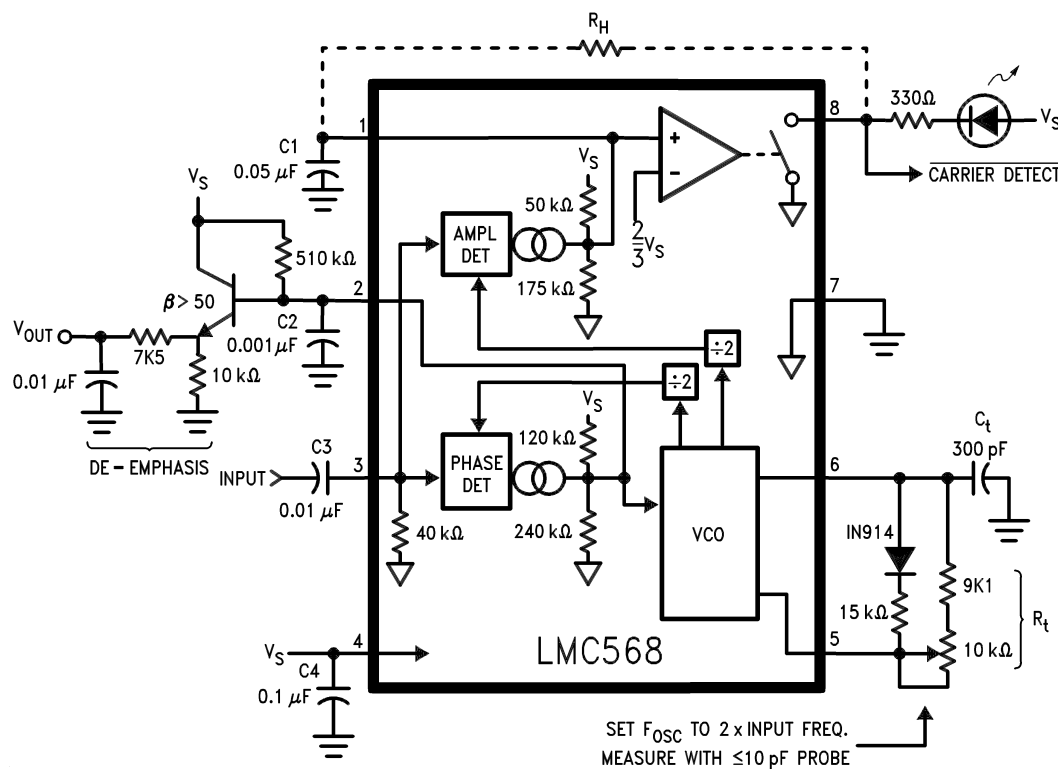
(100 kHz input frequency, refer to [Notes to Typical Application](#))


Figure 1. 8-Pin SOIC or PDIP
See D or P Package



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

All trademarks are the property of their respective owners.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings⁽¹⁾⁽²⁾

Input Voltage, Pin 3			2 V _{p-p}
Supply Voltage, Pin 4			10V
Output Voltage, Pin 8			13V
Voltage at All Other Pins			V _s to Gnd
Output Current, Pin 8			30 mA
Package Dissipation			500 mW
Operating Temperature Range (T _A)			-25°C to +125°C
Storage Temperature Range			-55°C to +150°C
Soldering Information	PDIP Package	Soldering (10 seconds)	260°C
	SOIC Package	Vapor Phase (60 seconds)	215°C
		Infrared (15 seconds)	220°C

- (1) "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits.
- (2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.

Electrical Characteristics

Test Circuit, T_A = 25°C, V_S = 5V, RtCt #2, Sw. 1 Pos. 0; and no input unless otherwise noted.

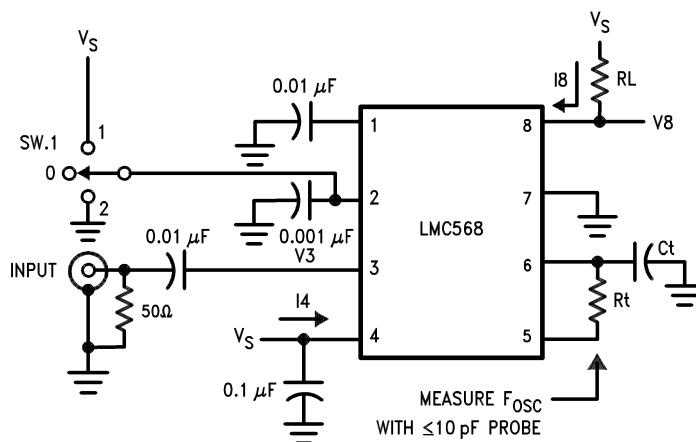
Symbol	Parameter	Conditions	Min	Typ	Max	Units
I ₄	Power Supply Current	RtCt # 1, Quiescent or Activated	V _S = 2V	0.35		mAdc
			V _S = 5V	0.75	1.5	
			V _S = 9V	1.2	2.4	
V ₃	Input D.C. Bias			0		mVdc
R ₃	Input Resistance			40		kΩ
I ₈	Output Leakage			1	100	nAdc
f ₀	Center Frequency F _{osc} ÷ 2	RtCt #2, Measure Oscillator Frequency and Divide by 2	V _S = 2V	98		kHz
			V _S = 5V	90	103	
			V _S = 9V		105	
Δf ₀	Center Frequency Shift with Supply	$\frac{f_{0 9V} - f_{0 2V}}{7 f_{0 5V}} \times 100$		1.0	2.0	%/V
V _{in}	Input Threshold	Set Input Frequency Equal to f ₀ Measured Above, Increase Input Level until Pin 8 Goes Low.	V _S = 2V	8	16	mVrms
			V _S = 5V	15	26	
			V _S = 9V		45	
ΔV _{in}	Input Hysteresis	Starting at Input Threshold, Decrease Input Level until Pin 8 Goes High		1.5		mVrms
V ₈	Output "Sat" Voltage	Input Level > Threshold Choose RL for Specified I ₈	I ₈ = 2 mA	0.06	0.15	Vdc
			I ₈ = 20 mA	0.7		
L.D.B.W.	Largest Detection Bandwidth	Measure F _{osc} with Sw. 1 in Pos. 0, 1, and 2; L.D.B.W. = $\frac{F_{osc P2} - F_{osc P1}}{F_{osc P0}} \times 100$	V _S = 2V	30		%
			V _S = 5V	40	55	
			V _S = 9V		60	
ΔBW	Bandwidth Skew	$Skew = \left(\frac{F_{osc P2} - F_{osc P1}}{2 F_{osc P0}} - 1 \right) \times 100$		1	±5	%
V _{out}	Recovered Audio	Typical Application Circuit Input = 100 mVrms, F = 100 kHz F _{mod} = 400 Hz, ± 10 kHz Dev.	V _S = 2V	170		mVrms
			V _S = 5V	270		
			V _S = 9V	400		

Electrical Characteristics (continued)

Test Circuit, $T_A = 25^\circ\text{C}$, $V_S = 5\text{V}$, RtCt #2, Sw. 1 Pos. 0; and no input unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
THD	Total Harmonic Distortion	Typical Application Circuit as Above, Measure V_{out} Distortion.		0.5		%
$\frac{S + N}{N}$	Signal to Noise Ratio	Typical Application Circuit Remove Modulation, Measure V_n ($S + N$)/ $N = 20 \log (V_{\text{out}}/V_n)$.		65		dB
f_{max}	Highest Center Freq.	RtCt #3, Measure Oscillator Frequency and Divide by 2		700		kHz

Test Circuit



RtCt	Rt	Ct
#1	100k	300 pF
#2	10k	300 pF
#3	5.1k	62 pF

Notes to Typical Application

SUPPLY DECOUPLING

The decoupling of supply pin 4 becomes more critical at high supply voltages with high operating frequencies, requiring C4 to be placed as close to possible to pin 4. Also, due to pin voltages tracking supply, a large C4 is necessary for low frequency PSRR.

OSCILLATOR TIMING COMPONENTS

The voltage-controlled oscillator (VCO) on the LMC568 must be set up to run at twice the frequency of the input signal. The components shown in the typical application are for $F_{osc} = 200$ kHz (100 kHz input frequency). For operation at lower frequencies, increase the capacitor value; for higher frequencies proportionally reduce the resistor values.

If low distortion is not a requirement, the series diode/resistor between pins 6 and 5 may be omitted. This will reduce VCO supply dependence and increase V_{out} by approximately 2 dB with THD = 2% typical. The center frequency as a function of R_t and C_t is given by:

$$F_{osc} \cong \frac{1}{1.4 R_t C_t} \text{ Hz} \quad (1)$$

To allow for I.C. and component value tolerances, the oscillator timing components will require a trim. This is generally accomplished by using a variable resistor as part of R_t , although C_t could also be padded. The amount of initial frequency variation due to the LMC568 itself is given in the electrical specifications; the total trim range must also accommodate the tolerances of R_t and C_t .

INPUT PIN

The input pin 3 is internally ground-referenced with a nominal 40 k Ω resistor. Signals that are centered on 0V may be directly coupled to pin 3; however, any d.c. potential must be isolated via C3.

OUTPUT TAKEOFF

The output signal is taken off the loop filter at pin 2. Pin 2 is the combined output of the phase detector and control input of the VCO for the phase-locked loop (PLL). The nominal pin 2 source resistance is 80 k Ω , requiring the use of an external buffer transistor to drive nominal loads.

For small values of C2, the PLL will have a fast acquisition time and the pull-in range will be set by the built-in VCO frequency stops, which also determine the largest detection bandwidth (LDBW). Increasing C2 results in improved noise immunity at the expense of acquisition time, and the pull-in range will become narrower than the LDBW. However, the maximum hold-in range will always equal the LDBW. The 2 kHz de-emphasis pole shown may be modified or omitted as required by the application.

CARRIER DETECT

Pin 1 is the output of a negative-going amplitude detector which has a nominal 0 signal output of $7/9 V_s$. The output at pin 8 is an N-channel FET switch to ground which is activated when the PLL is locked and the input is of sufficient amplitude to cause pin 1 to fall below $2/3 V_s$. The carrier detect threshold is internally set to 26 mVrms typical on a 5V supply.

Capacitor C1 in conjunction with the nominal 40 k Ω pin 1 internal resistance forms the output filter. The size of C1 is a tradeoff between slew rate and carrier ripple at the output comparator. Optional resistor R_H increases the hysteresis in the pin 8 output for applications such as audio mute control. The minimum allowable value for R_H is 330 k Ω .

LMC568 Typical Performance Characteristics

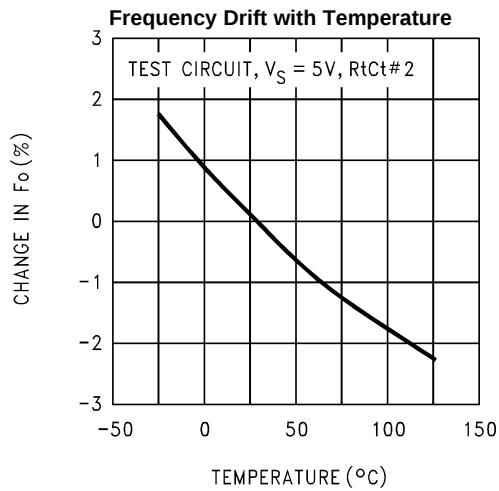


Figure 2.

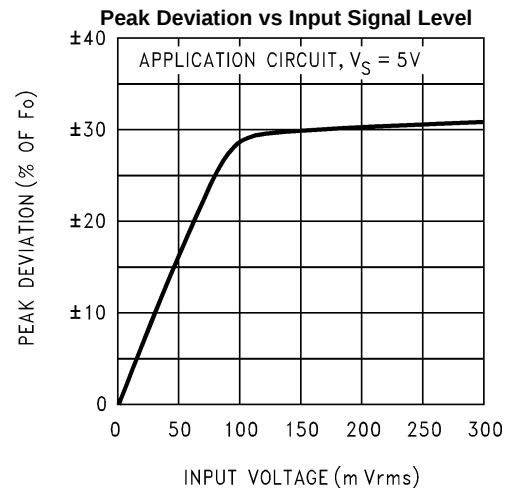


Figure 3.

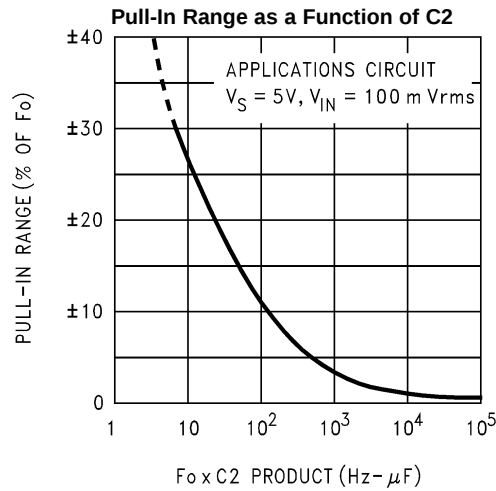


Figure 4.

REVISION HISTORY

Changes from Revision A (April 2013) to Revision B

Page

- Changed layout of National Data Sheet to TI format 5

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMC568CM/NOPB	LIFEBUY	SOIC	D	8		TBD	Call TI	Call TI	-25 to 100	LMC 568CM	
LMC568CMX/NOPB	LIFEBUY	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 0	LMC 568CM	

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

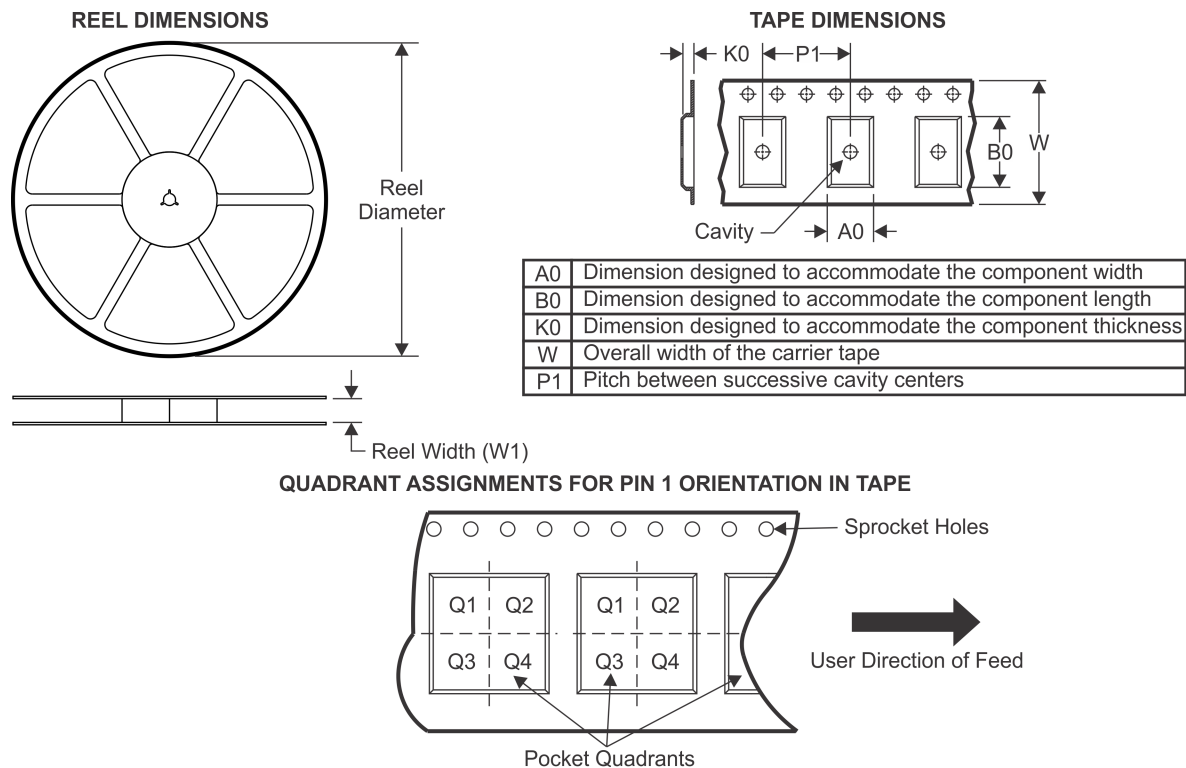
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

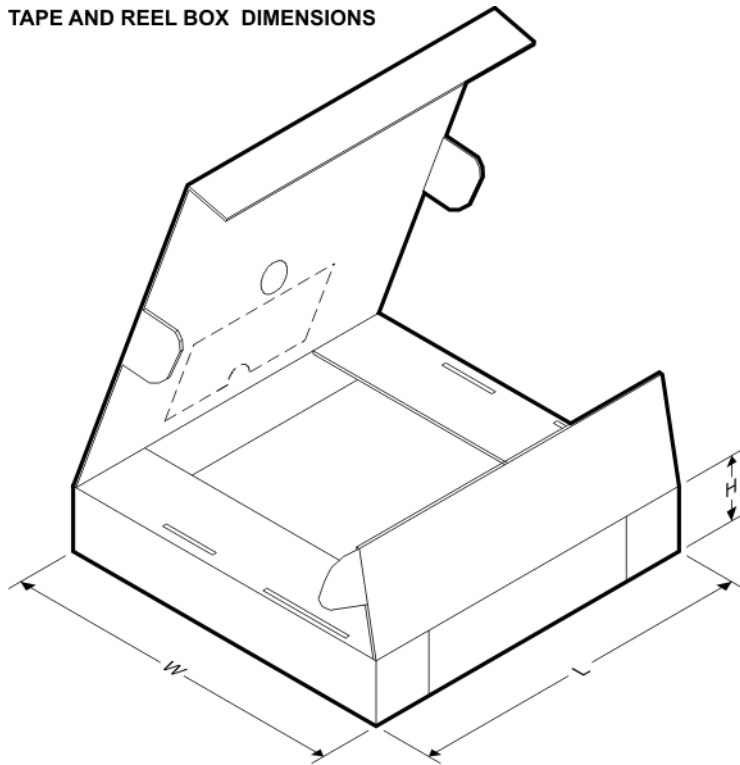
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMC568CMX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

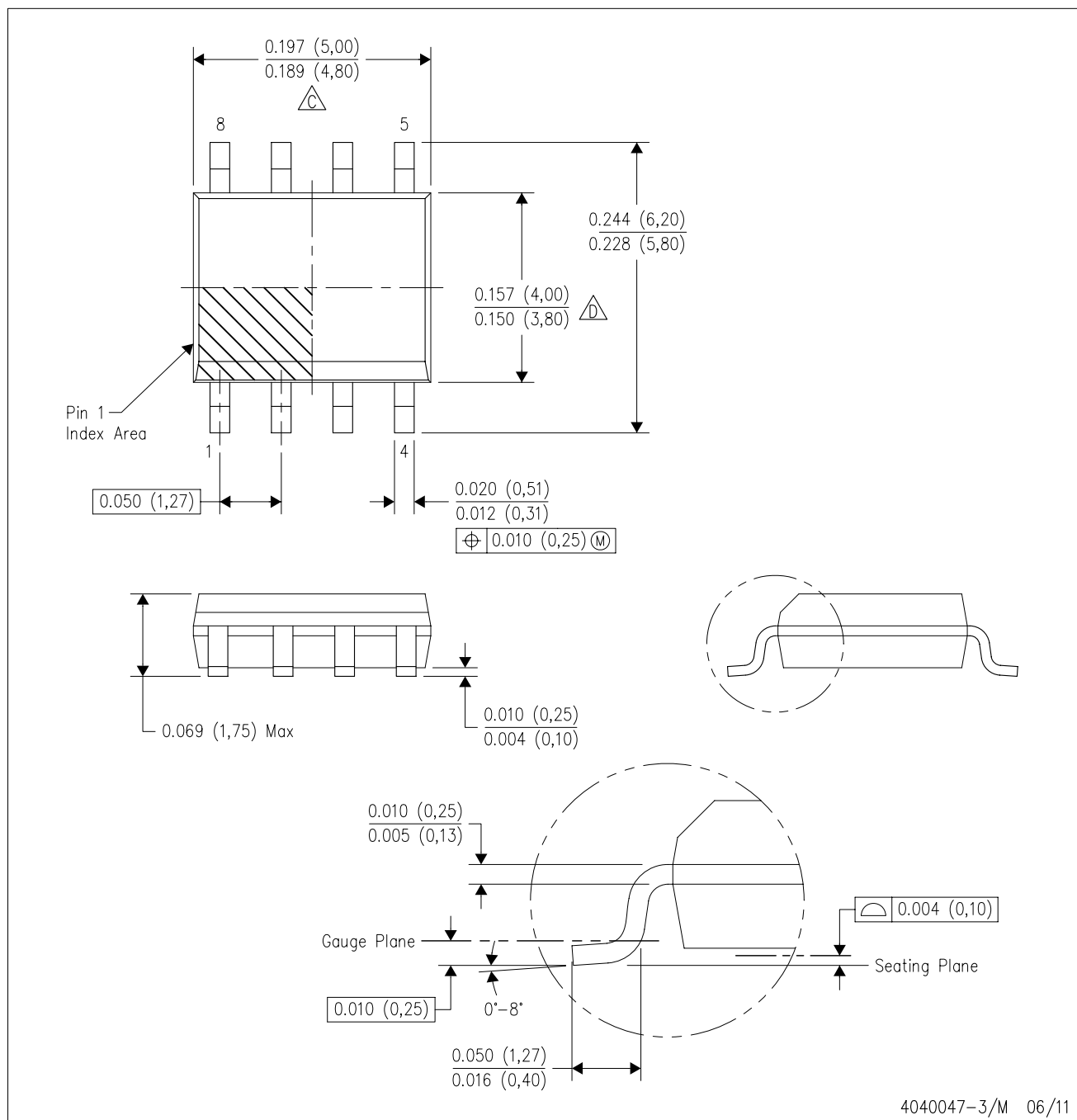


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMC568CMX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - $\triangle C$ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - $\triangle D$ Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AA.

IMPORTANT NOTICE

Texas Instruments Incorporated (TI) reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

TI's published terms of sale for semiconductor products (<http://www.ti.com/sc/docs/stdterms.htm>) apply to the sale of packaged integrated circuit products that TI has qualified and released to market. Additional terms may apply to the use or sale of other types of TI products and services.

Reproduction of significant portions of TI information in TI data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such reproduced documentation. Information of third parties may be subject to additional restrictions. Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyers and others who are developing systems that incorporate TI products (collectively, "Designers") understand and agree that Designers remain responsible for using their independent analysis, evaluation and judgment in designing their applications and that Designers have full and exclusive responsibility to assure the safety of Designers' applications and compliance of their applications (and of all TI products used in or for Designers' applications) with all applicable regulations, laws and other applicable requirements. Designer represents that, with respect to their applications, Designer has all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. Designer agrees that prior to using or distributing any applications that include TI products, Designer will thoroughly test such applications and the functionality of such TI products as used in such applications.

TI's provision of technical, application or other design advice, quality characterization, reliability data or other services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using TI Resources in any way, Designer (individually or, if Designer is acting on behalf of a company, Designer's company) agrees to use any particular TI Resource solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

Designer is authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY DESIGNER AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

Unless TI has explicitly designated an individual product as meeting the requirements of a particular industry standard (e.g., ISO/TS 16949 and ISO 26262), TI is not responsible for any failure to meet such industry standard requirements.

Where TI specifically promotes products as facilitating functional safety or as compliant with industry functional safety standards, such products are intended to help enable customers to design and create their own applications that meet applicable functional safety standards and requirements. Using products in an application does not by itself establish any safety features in the application. Designers must ensure compliance with safety-related requirements and standards applicable to their applications. Designer may not use any TI products in life-critical medical equipment unless authorized officers of the parties have executed a special contract specifically governing such use. Life-critical medical equipment is medical equipment where failure of such equipment would cause serious bodily injury or death (e.g., life support, pacemakers, defibrillators, heart pumps, neurostimulators, and implantables). Such equipment includes, without limitation, all medical devices identified by the U.S. Food and Drug Administration as Class III devices and equivalent classifications outside the U.S.

TI may expressly designate certain products as completing a particular qualification (e.g., Q100, Military Grade, or Enhanced Product). Designers agree that it has the necessary expertise to select the product with the appropriate qualification designation for their applications and that proper product selection is at Designers' own risk. Designers are solely responsible for compliance with all legal and regulatory requirements in connection with such selection.

Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer's non-compliance with the terms and provisions of this Notice.